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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,053	12/21/2001	Mark A. Burns	TI-33380	8705

7590

04/11/2003

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EXAMINER

NGUYEN, JIMMY

ART UNIT

PAPER NUMBER

2829

DATE MAILED: 04/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/026,053

Applicant(s)

BURNS, MARK A.

Examiner

Jimmy Nguyen

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Specification*

1. The specification is objected to because
  - page 20 line 4 test head 34/310/374 is not found. It should be 344/310/374Correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1- 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Maeng (US 6313652).

**As to claim 1**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC, comprising;

A first tester (test head 23 of figure 4) adapted to test the at least one first IC (on test tray 10) with a first test procedure (the first testing apparatus 100a);

A second tester (test head 23 of figure 4) adapted to test the at least one first IC ( on test tray 10 now move to the next location) with a second test procedure (the second testing apparatus 100b) simultaneously while the first tester (test head 23 of figure 4) tests the at least one second IC (new IC tray) with the first test procedure (the first testing apparatus 100a), wherein the first and second test procedures are adapted to test at least some different IC parameters (column 10 line 1 –5 ), wherein the first tester is coupled to the second tester (throughout the host computer 45); and

A single handler (40) coupled to the first and second testers.

**As to claims 2, 3**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC wherein the first tester (100a) is adapted to calibrate the second tester (100b) and the second tester (100b) is adapted to submit a request for calibration to the first tester.

**As to claim 4**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC wherein the first tester (100a) is adapted

to calibrate the second tester (100b) at predetermined time intervals or when ambient temperature has changed by a predetermined amount.

**As to claim 5**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC wherein the first test procedure comprises at least DC test (column 10 line 1 –5) and the second test procedure comprises at least thermal test (column 10 line 1 –5).

**As to claims 6, 7**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC wherein data transmittable (throughout the host computer 45) from the first tester (100a) to the second tester (100b) and /or from the second tester (100b) to the first tester (100a) and the host computer (45) perform as multiplexer.

**As to claims 8 -10**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC wherein IC from the wafer and testers comprise low and high cost testers.

**As to claim 11**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC wherein first IC that fail the first test procedures are moved to the second tester for testing with the second test

procedure. (if the IC in the test tray 10 fail from the testing apparatus 100a, the handler 40 will continue move those trays to process the new testing apparatus 100b).

**As to claim 12**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC comprising;

Control circuitry (45) coupled to the first tester (100a) and second tester (100b); and

Storage (50) means coupled to the control circuitry, first tester and second tester.

**As to claims 13 – 15**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC wherein first and second IC test procedure result information is storable in the storage with respect to first and second IC position and identification information (within the scope the invention).

**As to claims 16, 17**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC wherein the first tester (100a) is indirectly coupled to the second tester (100b) by a host computer (45) and they are integral.

**As to claims 18 – 20**, Maeng discloses (fig 5) an apparatus for testing at least one first IC and at least one second IC, comprising;

A first tester (test head 23 of figure 4) adapted to test the at least one first IC (on test tray 10) with a first test procedure (the first testing apparatus 100a);

A second tester (test head 23 of figure 4) adapted to test the at least one first IC ( on test tray 10 now move to the next location) with a second test procedure (the second testing apparatus 100b) simultaneously while the first tester (test head 23 of figure 4) tests the at least one second IC (new IC tray) with the first test procedure (the first testing apparatus 100a),

A single handler (40) coupled to the first and second testers; wherein the first (100a) and the second test (100b) procedures are adapted to test at least some different IC parameters (column 10 line 1- 5)

A first environmental chamber (32, see figure 4) coupled to the first tester (100a); and

A second environmental chamber (32, see figure 4) coupled to the second tester (100b), wherein the first and second test procedures comprise subjecting the first and second IC's to different environmental tests.

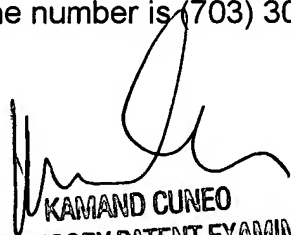
**As to claims 21 – 33**, the method for testing at least one first IC and at least one second IC are inherently within the Maeng's invention. This method claims are actually disclosed in figure 1 and 5 of Maeng.

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen at (703) 306-5858. Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4900.

JN.  
April 3, 2003

  
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